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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/817,215	04/02/2004	Xiang Zhu	M-15339 US	2417
7590	08/30/2005			EXAMINER TRA, ANH QUAN
Jon W. Hallman MacPHERSON KWOK CHEN & HEID LLP Suite 226 1762 Technology Drive San Jose, CA 95110			ART UNIT 2816	PAPER NUMBER
DATE MAILED: 08/30/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	10/817,215	ZHU ET AL. 
	Examiner	Art Unit
	Quan Tra	2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 02 April 2004.  
 2a) This action is FINAL.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-19 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-19 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
     1. Certified copies of the priority documents have been received.  
     2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
     3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- 1) Notice of References Cited (PTO-892)  
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
     Paper No(s)/Mail Date 4/2/04.
- 4) Interview Summary (PTO-413)  
     Paper No(s)/Mail Date. \_\_\_\_\_.  
 5) Notice of Informal Patent Application (PTO-152)  
 6) Other: \_\_\_\_\_.

## DETAILED ACTION

### *Drawings*

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-7, 14 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Abidin et al. (USP 6686794).

As to claim 1, Abidin et al. discloses in figure 1 a differential charge pump, comprising: a current switch (circuit on the left of 40) responsive to a pulse width difference between a differential up voltage (UP+, UP-) and a differential down voltage (DN+, DN-) to source and sink a current in a complementary fashion from a pair of differential output nodes (OUT+, OUT-)

), a first transconductance amplifier (41 in figure 4) configured to convert a voltage at a first one of the differential output nodes into a first current; and a second transconductance amplifier (42 in figure 5) configured to convert a voltage at a second one of the differential output nodes into a second current that is complementary to the first current.

As to claim 2, figure 5 shows a resistive load (43, 44) coupled between a first node and a second node, wherein the first transconductance amplifier is configured to couple the first current to the first node, and the second transconductance amplifier is configured to couple the second current to the second node.

As to claim 3, figures 1 and 5 show a common-mode feedback circuit (46 in figure 5 and I3, I5, I4, I8) configured to maintain a common-mode voltage on the resistive load equal to a common-mode reference voltage (CMFB).

As to claim 4, figure 5 shows that the first and second transconductance amplifiers are operational transconductance amplifiers.

As to claim 5, figure 1 shows that the current switch comprises: a first differential pair of transistors (21, 22) biased by a first current source (I1) to conduct the current, the transistors in the first differential pair being responsive to the differential up voltage such that when the differential up voltage is pulsed the current is conducted by a first transistor in the first differential pair and when the differential up voltage is not pulsed the current is conducted by a remaining second transistor in the first differential pair; and a second differential pair (23, 24) of transistors biased by a second current source (I2) to conduct the current such when the differential down voltage is pulsed the current is conducted by a first transistor in the second

differential pair and when the differential up voltage is not pulsed the current is conducted by a remaining second transistor in the second differential pair.

As to claim 6, figure 1-5 show that the common-mode feedback circuit includes a first current source (61, 71 in figure 2 or 91, 92 in figure 3) configured to source twice the current to a first node; and a second current source (91, 92 in figure 3) configured to source twice the current to a second node, wherein the first transistor in the first differential pair and the second transistor in the second differential pair couples to the first node through resistive loads (67, 72 or 93), and wherein the second transistor in the first differential pair and the first transistor in the second differential couples to the second node through resistive loads (93).

As to claim 7, figure 1 shows that the first and second transistors in the first and second differential pairs are NMOS transistors.

Claims 14 and 15 recite similar limitations of claims above. Therefore, they are rejected for the same reasons.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 8-13 and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's prior art figure 1 in view of Abidin et al. (USP 6686794).

The prior art figure 1 shows all limitations of the claims except for the detail of charge pump circuit 160. However, Abidin et al.'s figures 1-5 shows a differential charge pump circuit

that capable of operating in high speed. Therefore, it would have been obvious to one having ordinary skill in the art to use Abidin et al.'s charge pump for the charge pump in prior art figure 1 for the purpose of improving the operation speed of the circuit.

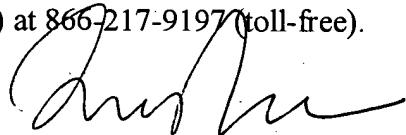
***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



QUAN TRA  
PRIMARY EXAMINER  
ART UNIT 2816

August 12, 2005